

Claims

I claim:

1. An interleaved clock generator for generating N interleaved clock signals in response to an input clock signal, the interleaved clock generator comprising:

interleaved clock generator means of a first type for receiving the input clock signal and for generating in response thereto M interleaved intermediate clock signals, the interleaved clock generator means of the first type including one of (a) a multi-stage serial-delay circuit and (b) a ring counter circuit; and

M interleaved clock generator means of a second type, each for receiving a respective one of the intermediate clock signals from the clock generator means of the first type and for generating in response thereto N/M of the N interleaved clock signals, each of the interleaved clock signal generator means of the second type including the other of (a) the multi-stage serial-delay circuit and (b) the ring counter circuit.

2. The interleaved clock generator of claim 1, in which the multi-stage serial-delay circuit includes a delay-locked loop.

3. The interleaved clock generator of claim 1, in which the multi-stage serial-delay circuit includes a phase-locked loop.

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4. The interleaved clock generator of claim 1, in which:
corresponding edges of temporally adjacent ones of the interleaved clock
signals differ in time by a time delay T_d ;
the interleaved clock signals have a frequency of $1/(N \times T_d)$;
5 the input clock signal has a frequency of $1/(M \times T_d)$ when the
interleaved clock generator means of the first type includes the multi-stage
serial delay circuit;
the input clock signal has a frequency of $M/(N \times T_d)$ when the
interleaved clock generator means of the first type includes the ring counter
circuit.
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5. The interleaved clock generator of claim 1, in which:
the interleaved clock generator means of the first type includes the
multi-stage serial-delay circuit; and
each of the interleaved clock signal generator means of the second type
5 includes the ring counter circuit.

6. The interleaved clock generator of claim 5, in which the ring counter
circuit includes an N/M -stage ring counter.

7. The interleaved clock generator of claim 5, in which the multi-stage
serial-delay circuit includes M delay stages, each providing one of the
intermediate clock signals.

8. The interleaved clock generator of claim 5, in which:
the input clock signal comprises differential clock signals each having a
50% duty cycle; and
the multi-stage serial-delay circuit includes $M/2$ delay stages, each
5 providing two of the intermediate clock signals.

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9. The interleaved clock generator of claim 1, in which:
the interleaved clock generator means of the first type includes the ring counter circuit; and
each of the interleaved clock signal generator means of the second type includes the multi-stage serial-delay circuit.

10. The interleaved clock generator of claim 9, in which the ring counter circuit includes an M-stage ring counter.

11. The interleaved clock generator of claim 9, in which the multi-stage serial-delay circuit includes N/M delay stages, each providing one of the interleaved clock signals.

12. The interleaved clock generator of claim 9, in which:
each intermediate clock signal comprises differential clock signals each having a 50% duty cycle; and
the multi-stage serial-delay circuit includes N/2M delay stages, each providing two of the interleaved clock signals.

13. An interleaved clock generator for generating N interleaved clock signals in response to an input clock signal, the interleaved clock generator comprising:

an interleaved clock generator of a first type, including a clock input connected to receive the input clock signal, M intermediate clock outputs, and one of (a) a multi-stage serial-delay circuit and (b) a ring counter circuit, the interleaved clock generator of the first type operating in response to the input clock signal to output a respective intermediate clock signal at each of the intermediate clock outputs; and

M interleaved clock generators of a second type, each including an intermediate clock input connected to a different one of the M intermediate clock outputs of the interleaved clock signal generator of the first type, N/M clock outputs and the other of (a) the multi-stage serial-delay circuit and (b) the ring counter circuit, each of the interleaved clock generators of the second type operating in response to the intermediate clock signal to output a respective one of N/M of the interleaved clock signals at each of the clock outputs.

14. The interleaved clock generator of claim 13, in which:

corresponding edges of temporally adjacent ones of the interleaved clock signals differ in time by a time delay T_d ;

the interleaved clock signals have a frequency of $1/(N \times T_d)$;

the input clock signal has a frequency of $1/(M \times T_d)$ when the interleaved clock generator of the first type includes the multi-stage serial delay circuit;

the input clock signal has a frequency of $M/(N \times T_d)$ when the interleaved clock generator of the first type includes the ring counter circuit.

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15. The interleaved clock generator of claim 13, in which:
the interleaved clock generator of the first type includes the multi-stage serial-delay circuit; and
each of the interleaved clock signal generators of the second type
5 includes the ring counter circuit.

16. The interleaved clock generator of claim 15, in which the ring counter circuit includes an N/M-stage ring counter.

17. The interleaved clock generator of claim 15, in which the multi-stage serial-delay circuit includes M delay stages, each providing one of the intermediate clock signals.

18. The interleaved clock generator of claim 13, in which:
the interleaved clock generator of the first type includes the ring counter circuit; and
each of the interleaved clock signal generators of the second type
5 includes the multi-stage serial-delay circuit.

19. An interleaved clock generator for generating N interleaved clock signals in response to an input clock signal, the interleaved clock generator comprising:

a multi-stage serial-delay circuit connected to receive the input clock signal, the multi-stage serial-delay circuit including M intermediate clock outputs; and

connected to each of the M intermediate clock outputs, a ring counter circuit that generates N/M of the N interleaved clock signals.

20. The interleaved clock generator of claim 19, in which the ring counter circuit comprises an N/M-stage ring counter.

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